Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently Amended) An improved high-speed adaptive equalizer device comprising:

one or more controllable analog filters comprising:

one or more data signal inputs for receiving one or more data signals;

one or more control signal inputs for receiving one or more control signals; and

one or more outputs for carrying filtered data signal output signals; and

one or more error generators for assessing the performance of one or more of said controllable analog filters according to one or more error functions coupled to one or more of said analog filters comprising:

one or more inputs for receiving one or more of said filtered data signal output signals from a controllable analog filter, wherein a weighting function is applied to [[a]] at least one of said filtered data signals output signal received from said controllable analog filter to emphasize a first portion of said filtered data signal output signal over a second portion of said filtered data signal output signal, said first portion corresponding to a middle point of a signal eye pattern representing signal amplitude versus time and said second portion corresponding to a zero crossing point of said signal eye pattern; and

one or more outputs for carrying error generator output data signals.

Claim 2. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more processing modules for processing said error generator output data signals creating processed data signals.

Claim 3. (Original) The improved high-speed adaptive equalizer device of claim 2 wherein one or more of said processing modules comprise one or more error acquisition blocks for applying one or more acquisition filters to one or more of said error generator output data signals thereby creating one or more processed signals coupled to one or more of said error generators comprising:

one or more inputs for receiving said error generator output data signals; and

one or more outputs for carrying processed data signals.

Claim 4. (Original) The improved high-speed adaptive equalizer device of claim 3 wherein one or more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a low pass filter or an integrator.

Claim 5. (Previously Presented) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more equalizer controllers for controlling one or more of said controllable analog filters according to one or more algorithms comprising:

one or more inputs for receiving equalizer controller input data signals; and

one or more outputs for carrying said control signals coupled to one or more of said control signal inputs.

Claim 6. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

Claim 7. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

Claim 8. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[3]]5 wherein one or more of said algorithms comprise a quasi-Newton, steepest descent or multivariate minimization algorithm.

Claim 9. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

Claim 10. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

Claim 11. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein said analog filter comprises one or more transversal filters, lattice filters, linear filters or non-linear filters.

Claim 12. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

Claim 13. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said control signal inputs comprise analog input or digital input.

Claim 14. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein said equalizer controller comprises one or more processing units, microprocessors, software modules, firmware modules or digital devices.

Claim 15. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein said equalizer controller further comprises one or more external data outputs.

Claim 16. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein said equalizer controller further comprises one or more external control signal outputs.

Claim 17. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]5 wherein said equalizer controller further comprises one or more external data inputs.

Claim 18. (Currently Amended) The improved high-speed adaptive equalizer device of claim [[1]]17 wherein said equalizer controller further comprises one or more external control signal inputs.

Claim 19. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said controllable analog filters further comprises one or more external data signal outputs.

Claim 20. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators further comprises one or more external data signal outputs.

Claim 21. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises one or more eye monitors.

Claim 22. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises a clock or clock recovery system.

Claim 23. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators is coupled to a clock or clock recovery system.

Claim 24. (Original) The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error generators comprises one or more weighting function modules.

Claim 25. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more modules comprising a capacity reporting module, a device status module, a link monitor or a monitoring module.

Claim 26. (Original) The improved high-speed adaptive equalizer device of claim 1 further comprising one or more modules comprising a joint optimization module, a chromatic dispersion module, a receiver gain module, a sampling phase module, a decision threshold level module or a DC offset module.

Claim 27. (Currently Amended) A method for improved high-speed adaptive equalization, said method comprising:

receiving one or more data inputs at one or more controllable analog filters;

filtering said one or more data inputs according to filter coefficients to create one or more filtered data signals;

receiving said filtered data signals at one or more error generators;

applying a weighting function ~~is applied~~ to [[a]] at least one of said filtered data signals to emphasize a first portion of said filtered data signal over a second portion of said filtered data signal, said first portion corresponding to a middle point of a signal eye pattern representing signal amplitude versus time and said second portion corresponding to a zero crossing point of said signal eye pattern; and

assessing the performance of one or more of said controllable analog filters according to one or more error functions creating one or more error generator output data signals.

Claim 28. (Currently Amended) The method of claim 27 further comprising providing one or more external data output signals after said filtering.

Claim 29. (Previously Presented) The method of claim 27 wherein said assessing the performance of one or more of said controllable analog filters further comprises applying a function to said filtered data signals comprising a normalization function or level shift function.

Claim 30. (Previously Presented) The method of claim 27 wherein said assessing the performance of one or more of said controllable analog filters further comprises applying one or more weighting functions to said error generator output data signals.

Claim 31. (Previously Presented) The method of claim 27 further comprising processing said error generator output signals creating processed data signals.

Claim 32. (Previously Presented) The method of claim 31 wherein said processing said error generator output signals comprises:

receiving said error generator output data signals at an error acquisition module; and

filtering said error generator output data signals according to one or more acquisition filters.

Claim 33. (Previously Presented) The method of claim 32 wherein said filtering said error generator output data signals according to one or more acquisition filters comprises processing said error generator output data signals with a filter comprising an anti-aliasing filter, a nose reduction filter, a low pass filter or an integrator.

Claim 34. (Previously Presented) The method of claim 32 further comprising digitizing said error generator output data signals.

Claim 35. (Previously Presented) The method of claim 27 further comprising:

receiving equalizer controller input data signals at an equalizer controller;

computing a new set of filter coefficients according to one or more error minimization algorithms; and

controlling one or more of said controllable analog filters by adjusting said filter coefficients to said new set of filter coefficients.

Claim 36. (Original) The method of claim 35 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

Claim 37. (Previously Presented) The method of claim 35 further comprising executing joint optimization with respect to one or more external devices.

Claim 38. (Previously Presented) The method of claim 35 further comprising assessing capacity, device status or link monitor status based on said filter coefficients.

Claim 39. (Previously Presented) The method of claim 38 further comprising reporting said capacity, device status or link monitor status based on said filter coefficients.

Claim 40. (Previously Presented) The method of claim 27 further comprising operating iteratively.

Claim 41. (Previously Presented) The method of claim 27 further comprising initializing one or more of said controllable analog filters to an initial setting comprising a set of said filter coefficients based on a pass-through mode, stored values or external input.

Claim 42. (Currently Amended) A system for improved optical networking comprising:

an improved high-speed adaptive equalizer device comprising:

one or more controllable analog filters comprising:

one or more data signal inputs for receiving one or more data signals;

one or more control signal inputs for receiving one or more control signals; and

one or more outputs for carrying filtered data signal output signals; and

one or more error generators for assessing the performance of one or more of said controllable analog filters according to one or more error functions coupled to one or more of said analog filters comprising:

one or more inputs for receiving one or more of said filtered data signal output signals from a controllable analog filter, wherein a weighting function is applied to [[a]] at least one of said filtered data signal output signals received from said controllable analog filter to emphasize a first portion of said filtered data signal output signal over a second portion of said filtered data signal output signal, said first portion corresponding to a middle point of a signal eye pattern representing signal amplitude versus time and said second portion corresponding to a zero crossing point of said signal eye pattern; and

one or more outputs for carrying error generator output data signals.

Claim 43. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer further comprises one or more processing modules for processing said error generator output data signals creating processed data signals.

Claim 44. (Original) The system of claim 43 wherein one or more of said processing modules comprise one or more error acquisition blocks for applying one or more acquisition filters to one or more of said error generator output data signals thereby creating one or more processed signals coupled to one or more of said error generators comprising:

one or more inputs for receiving said error generator output data signals; and

one or more outputs for carrying processed data signals.

Claim 45. (Previously Presented) The system of claim 44 wherein one or more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a low pass filter or an integrator.

Claim 46. (Previously Presented) The system of claim 42 wherein said improved high-speed adaptive equalizer further comprises one or more equalizer controllers for controlling one or more of said controllable analog filters according to one or more algorithms comprising:

one or more inputs for receiving equalizer controller input data signals; and

one or more outputs for carrying said control signals coupled to one or more of said control signal inputs.

Claim 47. (Currently Amended) The system of claim [[42]]46 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

Claim 48. (Original) The system of claim 42 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

Claim 49. (Currently Amended) The system of claim [[44]]46 wherein one or more of said algorithms comprise a quasi-Newton, steepest descent or multivariate minimization algorithm.

Claim 50. (Currently Amended) The system of claim [[42]]46 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

Claim 51. (Original) The system of claim 42 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

Claim 52 (Original) The system of claim 42 wherein said analog filter comprises one or more transversal filters, lattice filters, linear filters or non-linear filters.

Claim 53. (Original) The system of claim 42 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

Claim 54 (Original) The system of claim 42 wherein one or more of said control signal inputs comprise analog input or digital input.

Claim 55. (Currently Amended) The system of claim [[42]]46 wherein said equalizer controller comprises one or more processing units, microprocessors, software modules, firmware modules or digital devices.

Claim 56. (Currently Amended) The system of claim [[42]]46 wherein said equalizer controller further comprises one or more external data outputs.

Claim 57. (Currently Amended) The system of claim [[42]]46 wherein said equalizer controller further comprises one or more external control signal outputs.

Claim 58. (Currently Amended) The system of claim [[42]]57 wherein said equalizer controller further comprises one or more external data inputs.

Claim 59. (Cancelled)

Claim 60. (Original) The system of claim 42 wherein one or more of said controllable analog filters further comprises one or more external data signal outputs.

Claim 61. (Original) The system of claim 42 wherein one or more of said error generators further comprises one or more external data signal outputs.

Claim 62. (Original) The system of claim 42 wherein one or more of said error generators comprises one or more eye monitors.

Claim 63. (Original) The system of claim 42 wherein one or more of said error generators comprises a clock or clock recovery system.

Claim 64. (Original) The system of claim 42 wherein one or more of said error generators is coupled to a clock or clock recovery system.

Claim 65. (Original) The system of claim 42 wherein one or more of said error generators comprises one or more weighting function modules.

Claim 66. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer device further comprises one or more modules comprising a capacity reporting module, a device status module, a link monitor or a monitoring module.

Claim 67. (Original) The system of claim 42 wherein said improved high-speed adaptive equalizer device further comprises one or more modules comprising a joint optimization module, a chromatic dispersion module, a receiver gain module, a sampling phase module, a decision threshold level module or a DC offset module.